

PCTWORLD INTELLECTUAL PROPERTY ORGANIZATION
International Bureau

INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 6 : H01L 31/0203, 27/146, 27/16	A1	(11) International Publication Number: WO 95/17014 (43) International Publication Date: 22 June 1995 (22.06.95)
(21) International Application Number: PCT/US94/14335 (22) International Filing Date: 12 December 1994 (12.12.94) (30) Priority Data: 08/166,492 13 December 1993 (13.12.93) US (71) Applicant: HONEYWELL INC. [US/US]; Honeywell Plaza, Minneapolis, MN 55408 (US). (72) Inventors: HIGASHI, Robert, E.; 20220 Manor Road, Shorewood, MN 55331 (US). RIDLEY, Jeffrey, A.; 13021 Highpoint Curve, Burnsville, MN 55337 (US). STRATTON, Thomas, G.; 3000 Sandy Hook Drive, Roseville, MN 55113 (US). (74) Agent: MCDOWALL, Paul, H.; Honeywell Inc., Honeywell Plaza - MN12-8251, Minneapolis, MN 55408 (US).		(81) Designated States: CA, JP, European patent (AT, BE, CH, DE, DK, ES, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE). Published <i>With international search report.</i>
(54) Title: INTEGRATED SILICON VACUUM MICROPACKAGE FOR INFRARED DEVICES		
(57) Abstract <p>An efficient method brings together two wafers of dies that contain an infrared transparent window or top cap with either an infrared detector or emitter array to produce a low cost infrared package. A low thermal conductivity gas or a vacuum may be used between the wafers for enhanced thermal isolation. Joining of the wafers is preferably by solder, although ultrasound bonding can be used.</p>		

FOR THE PURPOSES OF INFORMATION ONLY

Codes used to identify States party to the PCT on the front pages of pamphlets publishing international applications under the PCT.

AT	Austria	GB	United Kingdom	MR	Mauritania
AU	Australia	GE	Georgia	MW	Malawi
BB	Barbados	GN	Guinea	NE	Niger
BE	Belgium	GR	Greece	NL	Netherlands
BF	Burkina Faso	HU	Hungary	NO	Norway
BG	Bulgaria	IE	Ireland	NZ	New Zealand
BJ	Benin	IT	Italy	PL	Poland
BR	Brazil	JP	Japan	PT	Portugal
BY	Belarus	KE	Kenya	RO	Romania
CA	Canada	KG	Kyrgyzstan	RU	Russian Federation
CF	Central African Republic	KP	Democratic People's Republic of Korea	SD	Sudan
CG	Congo	KR	Republic of Korea	SE	Sweden
CH	Switzerland	KZ	Kazakhstan	SI	Slovenia
CI	Côte d'Ivoire	LI	Liechtenstein	SK	Slovakia
CM	Cameroon	LK	Sri Lanka	SN	Senegal
CN	China	LU	Luxembourg	TD	Chad
CS	Czechoslovakia	LV	Latvia	TG	Togo
CZ	Czech Republic	MC	Monaco	TJ	Tajikistan
DE	Germany	MD	Republic of Moldova	TT	Trinidad and Tobago
DK	Denmark	MG	Madagascar	UA	Ukraine
ES	Spain	ML	Mali	US	United States of America
FI	Finland	MN	Mongolia	UZ	Uzbekistan
FR	France			VN	Viet Nam
GA	Gabon				

INTEGRATED SILICON VACUUM MICROPACKAGE FOR INFRARED DEVICES

This application relates to the field of infrared sensing and infrared scene projection or emission, and particularly to the packaging of arrays of small elements thereof.

BACKGROUND

Thermal isolation is very important for thermal based infrared devices (detector or emitters), as opposed to quantum sensors or emitters, since the detection or transmission of infrared radiation is directly related to the temperature rise achieved by the detector or emitters of the device. The better the thermal isolation of the detector or emitters the more efficient the device will be at converting radiation to heat (detector) or heat to radiation (emitter). Vacuum packaging is a very effective means to improve performance. It reduces heat flow from individual infrared units to their neighbors and/or to surrounding surfaces via ambient gas molecules by eliminating such molecules.

Because microstructure infrared detector and emitter arrays are very small and fragile, common silicon production and packaging techniques may not be suitable for large scale production of these array bearing devices. Typical infrared units in the arrays are built to be thermally isolated from the chip, as well as their neighbors, thus having elements suspended apart from the substrate to enhance the thermal isolation by having the minimal physical contacts possible. These bridges or suspension structures can be particularly fragile, therefore the method of encapsulating them into a vacuum can be critical to device yield rates.

A method for packaging the die in a batch process substantially improves the yield, reduces the cost and at the same time achieves maximum performance of these devices. This type of packaging is necessary to mass produce low cost, thermally based infrared devices. The proposed package is termed a "micropackage."

Maintaining an effective vacuum in a sealed package is often challenging due to surface outgassing. Frequently heat treatments will minimize this but such outgassing determines the effective life of the device unless it can be periodically or continuously removed. Integrating a getter into each discrete chip would be a method of maintaining a good vacuum for all chips as the getter will counteract the outgassing generated by the package surfaces.

-2-

The innovative structures taught here provide tremendous cost savings over prior designs for packaging these devices, the capability of achieving much smaller packages, as well as having the potential to greatly increase packaged device yield for lower cost.

BRIEF DESCRIPTION OF THE DRAWINGS

5 Fig. 1 is a plan view of a wafer level design employed by a preferred embodiment of the invention.

 Fig. 2 is a cut-away side view at the wafer level in accord with a preferred embodiment of the invention.

10 Fig. 3 is a cut-away side view of an individual device of one preferred embodiment chip of the invention.

 Fig. 4 is a cut-away side view of another preferred embodiment chip of the invention.

 Fig. 5 is side view of two major components at the chip level of a preferred embodiment of the invention.

15 Fig. 6 is a top view of the surface patterning of the substrate layer (upper surface) at the chip level of a preferred embodiment of the invention.

SUMMARY OF THE INVENTION

A construction technique and infrared device built thereby are described herein.

20 A wafer assembly having infrared devices (which can be detectors or emitters, either singly or in an array or arrays) provide for an inexpensive way of packaging infrared devices. The wafer is covered and maintained in a vacuum by a top cap of infrared transparent material spaced apart therefrom by a solder bead and farther from the structure of the top cap wafer in some instances.

25 In either case, the result is a minimally thermoconductive space between the top cap and the infrared devices, which can be evacuated or filled with minimally thermoconductive fluid. The spacing can be provided by any or all of the solder bead; a recess in the top cap or an additional spacer layer of material added either to the bottom of the top cap or the upper surface of the infrared containing wafer.

30 In the preferred embodiment, the wafer assembly is then diced into its final chip components, each maintaining individual vacuum integrity. It is preferred that each vacuum cavity have an integral getter to increase the vacuum life of the component.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

Referring first to Fig. 1, a wafer which will be used to create a set of devices in accord with a preferred embodiment of the invention is shown, being a wafer composed of many devices or chips 8, constructed thereon by prior processes not described here.

5 In Fig. 2, a cross-sectional view is taken of a wafer like 7 of Fig. 1, having a top cap wafer (9b) attached thereto. The top cap wafer (9b) should be an IR transparent wafer. When attached in a vacuum, all the devices on one wafer are simultaneous sealed by the cap, in a highly efficient batch fabrication technique. The spacer material 11 both holds the wafers 9 and 9b apart and seals each individual chip or die 8, in its own area. The dotted lines around 84 show where the paired wafers would be diced to produce a chip based on the infrared device in area 84

Referring now to Fig. 3, a device in accord with the preferred embodiment 10 is illustrated at the "device" or chip level, having two major component parts; a substrate or base chip 9 and a top cover 12. On the surface of the top cover 12 is an anti-reflective layer 13 and underneath its surface is a second anti reflective coating 14. (Substances used for anti-reflective coatings are well known.) The joining of the two halves in accord with this invention yields a space 21 between them. By sealing them together, preferably with a solder layer 16, 16a while the two halves are in a vacuum, the cavity 21 itself remains evacuated. The solder layer can be applied by vacuum deposition and either lift-off or etch, or by masking and plating. The wafer or chip containing the microbolometers 20 and or other type (pyroelectric, thermoelectric, etc.) of thermal infrared sensitive devices, are manufactured first. Such manufacture is not a part of this patent and can be done in numerous known ways. There can be electronics 25 beneath the surface layer that provides some signal processing and/or switching properties which the infrared sensitive devices (20) will use. Generally, there is a layer 22 of electrical connections and the microbolometer 22a or other infrared sensitive or emitting devices. These electrical leads can be passivated (i.e., coated with a protective layer of material, for example, silicon nitride or other well known passivation material) such that the solder layer can be applied over them and form the vacuum seal without shorting the leads together. The leads terminate on pads 18 that wire bonds can be made on and connected to other circuitry off the infrared sensitive device.

-4-

The infrared sensitive elements 20 are usually thin film structures that are suspended above the chip surface for thermal isolation and such devices are very fragile in subsequent manufacturing steps. Figure 3 illustrates devices where this thermal isolation is accomplished by etching away part of the substrate 22b. The top cap needs to be separated from the thermally isolated elements so as to not touch the elements and conduct heat towards or away from the elements. An effective way to assure a good cavity size is to etch a recess in the top cap surface 15. With this etching done, when the solder is molten and the wafers are pressed together, extreme measures are not necessary to prevent the solder from being squeezed out, causing the separation between pads 15a and 16 could become extremely small where the top cap is etched back, even with poor processing the cavity will be maintained. A metal layer 15a that the solder can wet to and to allow for the solder 16, 16a to be patterned on the top cap surface so as to form a ring or frame large enough to encircle the array of thermally isolated structures 20. A similar ring or frame of metal that the solder can wet to may also be preferably created on the wafer of detector/emitter die.

Two wafers are brought together in vacuum, using suitable wafer bonding equipment. Low levels of heat may be used for this processing step (solder usually reflows between 100-300 °C depending on type used, we presently prefer to use 50:50 InPb. The user may, of course, use any solder he/she prefers.) The die are sealed in vacuum and the fragile thermally isolated elements are protected from damage and debris associated with subsequent wafer sawing and die handling by the surrounding solder bead. Lines for wafer sawing 27, illustrate in one direction how die would be separated while maintaining the integrity of solder seal. (The top cap 12 should also have had its anti reflective layers 13 and 14 placed thereon before the joining of the two halves 12 and 11.)

Because the resultant package is only the thickness of two silicon wafers the result is a significant reduction in both the size and the weight of the package as compared to a standard vacuum package for similar devices. This aspect is important and desirable for almost all applications of infrared devices.

To ensure a low pressure is maintained within a micropackage (chip level vacuum cavity 21), it is useful to ensure that no materials which will excessively outgas lie within the micropackage. In addition, since the internal surfaces of the infrared die

-5-

and overlying window or top cap will have at least a small outgassing rate, it may be necessary, or at least useful, to include small quantities of a specialized getter material within the micropackage. The function of the getter material is to absorb outgassants, which would otherwise cause an increase in the internal pressure of the micropackage and the resulting decrease of the thermal isolation of the IR detector or emitter elements.

Suitable getter materials are well known, such as thin films of barium, vanadium, iron, zirconium or their alloys. Before such materials can act as getters, they must be activated by heating to a high temperature for a short period.

To incorporate and activate small quantities of getter materials within a micropackage, the required mass of getter material may be deposited monolithically upon suitable regions of the infrared die or the top cap. Numerals 23 and 24 show locations where such monolithic getters may preferably be placed. The getter material may be either deposited directly upon these surfaces 24, or upon thermally isolated microbridges 23 of such materials as silicon nitride. An advantage of deposition upon a microbridge is that the thermal isolation property of the microbridge allows thermal activation of the getter material by a small heating power applied for a short time, for example by an electrical heating current or a beam of heating radiation as produced by an infrared laser, without requiring the adjacent parts of the infrared die or window to be heated significantly.

If the getter is on a thermally isolated structure, an alternate heating method may be the supply of an electric current passed through a resistive heating element fabricated on the structure to heat the structure enough to activate the getter. To get electric power to the heater another solder pattern 23c can be produced at the same time as the solder ring 16, 16a to connect pads on the top cap 23a to pads on the device chip 23b. These pads 23b consist of a metal that solder can wet to and connect to leads 22 which will connect to pads 18 for wire bonding. A hole through the wafer 26 over the pads allows access to the sealed devices for wirebonding. If desired, a large molecule or atomic gas, preferably non-reactive such as Xenon, maybe used instead of the vacuum or vacuum/getter filler. Xenon is known, for example, to be only one-fifth as thermally conductive as air. Currently, the evacuated space and getter combination is preferred, however.

-6-

For lowest cost the top cap 12 should preferably be comprised of single crystal silicon, with low absorption in the region of infrared detection or emission. This is material which is transparent to infrared radiation and easily obtainable. Alternatively a window in the top cap wafer, or the top cap wafer itself, could be formed of a thin film of polycrystalline silicon or other materials such as germanium, GaAs, etc. with different degrees of transparency. Thus, if the structures at 20 are emitting structures, the infrared can be transmitted through the top cap 12 and, if they are receiving or detector structures, the infrared from the environment can be received into them also through top cap 12.

Referring now to Fig. 4, a substrate with infrared sensitive devices 44 is indicated by the numeral 41 and the device overall by the numeral 40. For very large arrays of infrared sensitive devices or thin windows in the top cap, the load of atmospheric pressure on the top cap and device chip can cause bowing such that the two inner surfaces can touch. At least one support post 43 may be added to cause the top cap to remain separated from the top cap 42 which in this embodiment is lengthened substantially without increasing its width. This permits for the encapsulation of very large arrays or infrared sensitive structures which are substantially more useful in infrared imaging devices, such as cameras, for instance. Figure 4 also shows another method that the top cap can be spaced apart from the thermally isolated elements. A standoff 45 of deposited material such as a metal can be patterned at the same time as the support post 43 thereby eliminating the need for the recess etch in the top cap surface. If desired, a metal that the solder can wet to can be patterned on top of the post for subsequent soldering operations.

In another alternative the getter could be placed on a thermally isolated structure on the detector/emitter die 47. Electrical connections to this getter for heating can be made as in the structure depicted in figure 3 with layers such as 22 and pads 18.

To further integrate the electronic portion of the system, electronic devices 48 could be fabricated in the top cap wafer and connections can be made to these devices in the same manner as the thermally isolated getter in figure 3 with pads 23a, 23b, solder 23c. Some of the benefits of placing electronics in the top cap are further size reduction, lower electrical noise due to shorter leads, and temperature matched very closely to the infrared sensitive die.

-7-

A layer of solder is preferable to all other structures known for this kind of bonding in a vacuum environment. However, ultrasonic pressure devices may also be used if properly constructed to push the entire post or pedestal structure against the surface of substrate 41 all at the same time.

5 A simple representation of the structure 30 is found in Fig. 5. In this case, a gap or hole 33 is made (in this case by etching) to provide for direct access to the bonding pads so that the infrared structures in substrate 31 (not shown) can have electrical access to the outside world. A layer of solder 34 is shown located on the underside of top cap 32 showing where such a solder layer might be located in a cold form for one preferred
10 form of assembly.

 Referring now to Fig. 6, the areas 51 through 59d of interest are illustrated on a surface 31. In the center of the set of structures is the area 51 in which the infrared sensitive structures would be located. Area 52 indicates the region in which the top cap cavity edge would be located. Beyond this is area 53 in which the solder layer such as
15 that shown in Fig. 5 (numeral 34) would be located. The outer edge 54 is also shown. Wire bonding pads 58a through 59d are shown within area 54. Area 55 describes the opening 33 as it may be situated when wafers or dies 31 and 32 are brought together for bonding. Thus, the bonding pads 58a through 59d would be available through opening 33.

CLAIMS

1. An infrared detector vacuum package characterized by a wafer having infrared detector units built thereon in an infrared detector array and a top cap wafer of infrared transparent material sealingly spaced apart from said infrared detector array by a
5 patterned solder layer.
2. An infrared emitter package characterized by a die having infrared emitter units built thereon in an infrared emitter array and a top cap wafer of infrared transparent material sealingly spaced apart from said infrared emitter array by a patterned solder
10 layer.
3. An infrared emitter vacuum package characterized by a die having an infrared emitter array thereon and a top cap wafer sealing said infrared emitter array into a cavity formed by the sealing of said die and said top cap.
15
4. A package according to claim 1, 2 or 3 wherein the space enclosed between the top cap and the infrared array is evacuated.
5. An infrared detector vacuum package characterized by a die having infrared
20 detector arrays thereon and a top cap wafer sealing said infrared detector array into a evacuated cavity formed by the sealing of said die and said top cap.
6. A package according to any preceding claim wherein said top cap and detector array are further spaced apart by a recess etched into the top cap.
25
7. A package according to any preceding claim wherein said top cap and detector array are further spaced apart by a spacer layer.
8. A package according to any of claims 1 to 3, 6 or 7 wherein the space enclosed
30 between the top cap and the infrared array is filled with a low thermal conductivity gas.
9. A package according to claim 8 wherein the gas is Xenon or Argon.

10. A package according to claim 8 or 9 having a getter situated monolithically in the top cap.
- 5 11. A package according to claim 8, 9 or 10 having a getter located monolithically in a suitable region of the area of said infrared array.
- 10 12. A package according to any preceding claim further comprising electronics means integrated into the top cap wafer for driving the infrared array to detect or emit infrared radiation.
- 15 13. A package according to any preceding claim further comprising a gap formed in the top cap wafer, and a metallic lead disposed therein providing electrical communication to the infrared array.
- 20 14. A package according to any preceding claim wherein the infrared detector unit or units comprise one or more semiconductor microbridge microstructures, each suspended above a cavity etched in the wafer.
- 25 15. A process of making infrared array packages from two wafers comprising:
 - a) evacuating a chamber contained by a top cap wafer having top cap dies and also containing an array wafer having array dies located so as to be pairable with said top cap dies;
 - b) physically bringing together the two wafers such that the paired arrays and the top caps are positioned so as to be sealable together;
 - c) sealing said wafers together;
 - d) dicing the paired dies.
- 30 16. A process according to claim 15 wherein solder is applied to either the top cap wafer or the array wafer at some time prior to step c).

-10-

17. A process according to claim 15 or 16 wherein the chamber is filled with a low thermal conductivity gas before step c).

18. A process according to any of claims 15 to 17 wherein the sealing step employs
5 ultrasonic bonding.

1/4

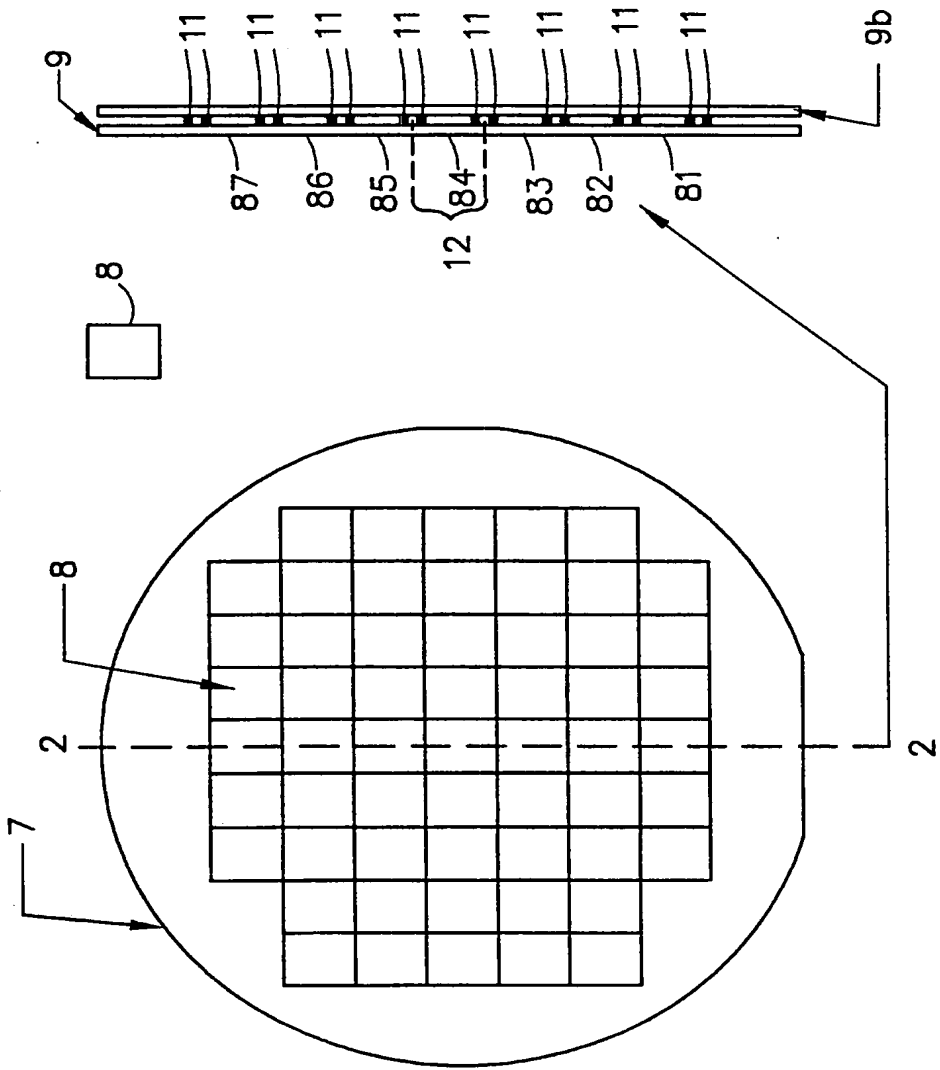


Fig 2

Fig 1

2/4

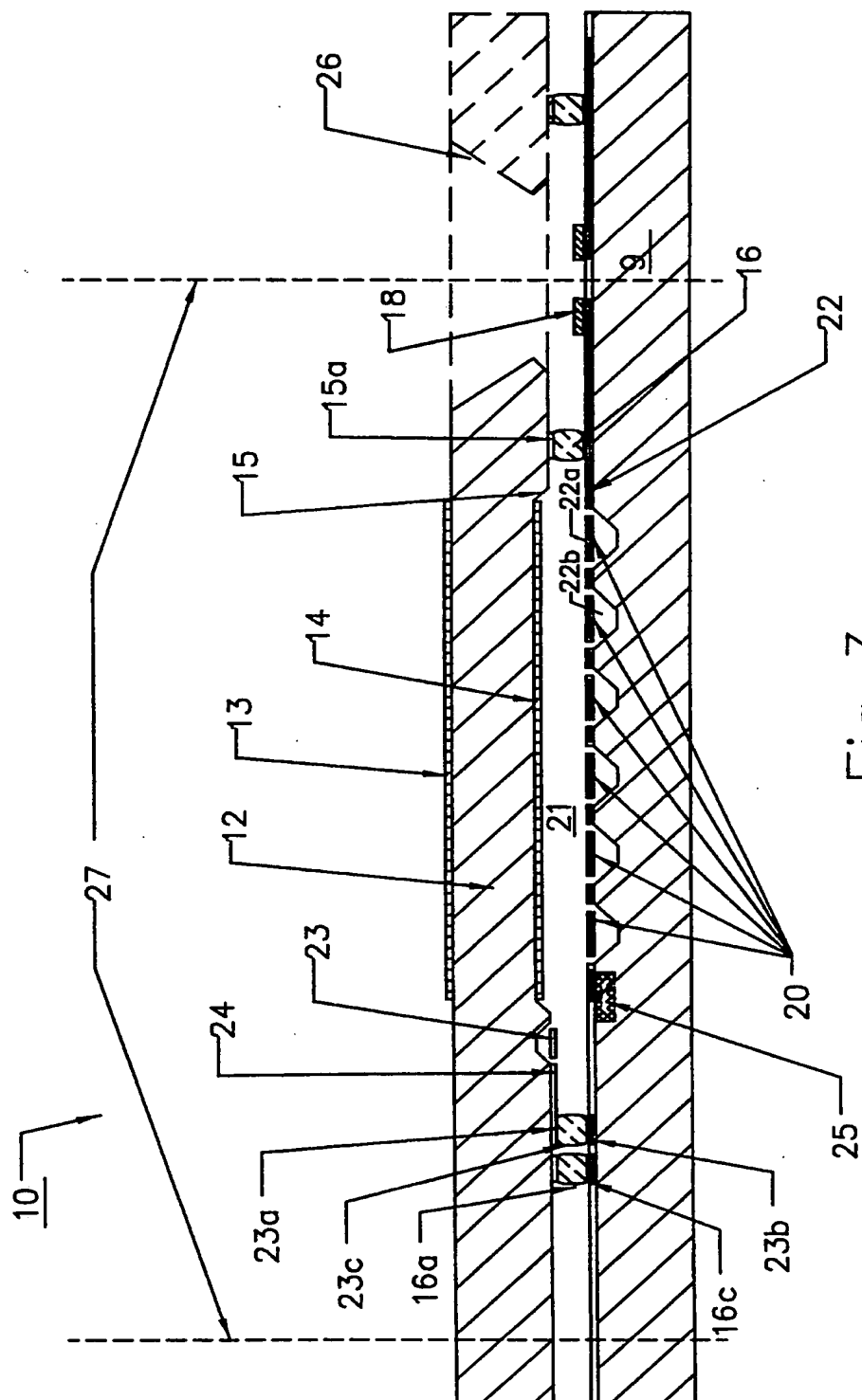


Fig 3

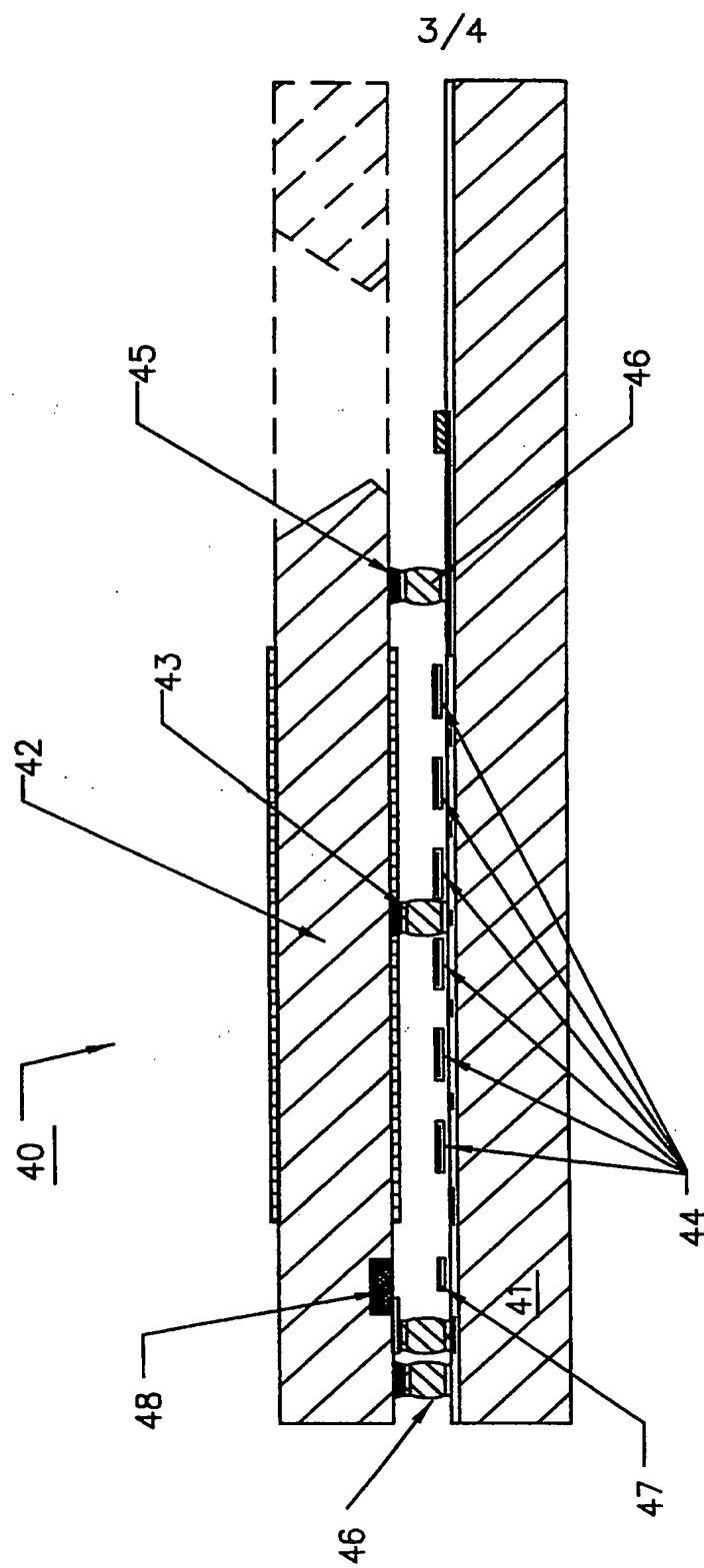


Fig 4

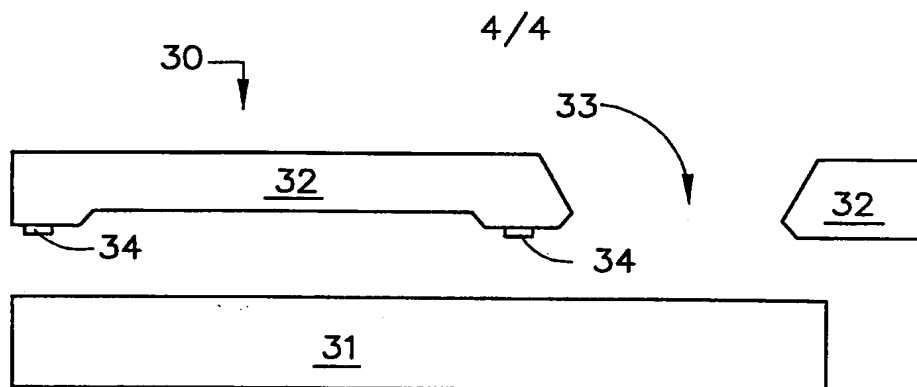


Fig. 5

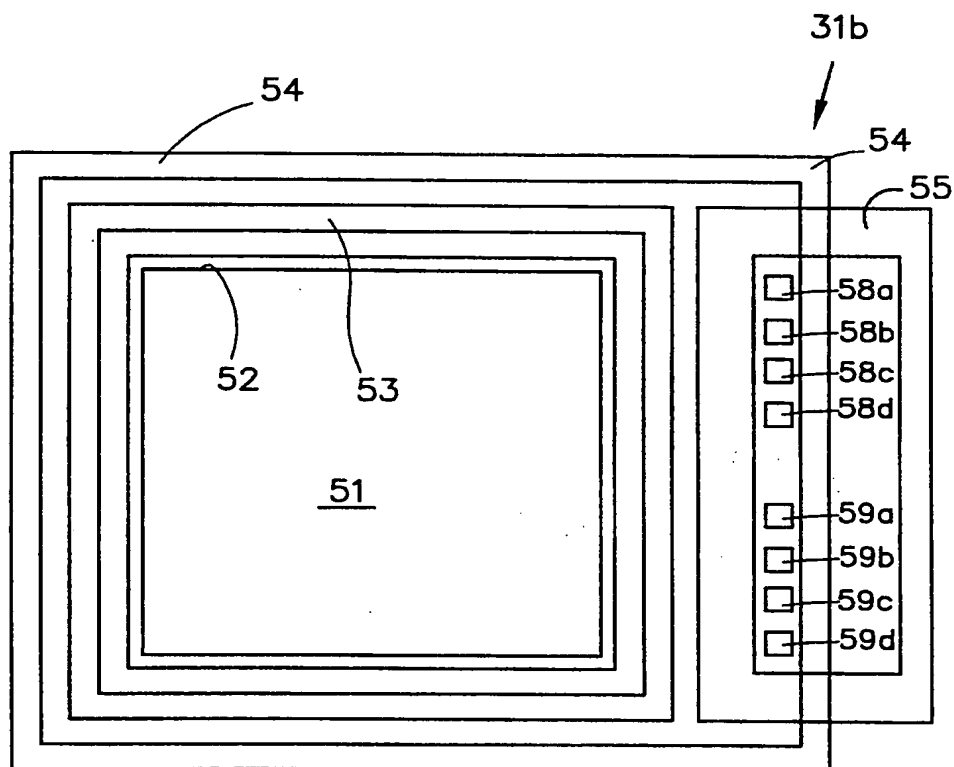


Fig. 6

INTERNATIONAL SEARCH REPORT

Inter nal Application No
PCT/US 94/14335

A. CLASSIFICATION OF SUBJECT MATTER

IPC 6 H01L31/0203 H01L27/146 H01L27/16

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC 6 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	GB,A,2 121 598 (MARCONI CO LTD) 21 December 1983 see page 1, line 108 - line 123 ----	1-5,8,9, 15
A	US,A,3 973 146 (ARNOLD EMIL ET AL) 3 August 1976 see the whole document ----	1,5
A	EP,A,0 453 372 (TERUMO CORP) 23 October 1991 see column 8, line 23 - line 33 ----	1,5,8,9
A	US,A,5 006 711 (HAMASHIMA SHIGEKI ET AL) 9 April 1991 see the whole document -----	1,5

☐ Further documents are listed in the continuation of box C.☒ Patent family members are listed in annex.

* Special categories of cited documents :

- "A" document defining the general state of the art which is not considered to be of particular relevance
- "E" earlier document but published on or after the international filing date
- "L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
- "O" document referring to an oral disclosure, use, exhibition or other means
- "P" document published prior to the international filing date but later than the priority date claimed

- "T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
- "X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
- "Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.
- "&" document member of the same patent family

Date of the actual completion of the international search

1 March 1995

Date of mailing of the international search report

16.03.95

Name and mailing address of the ISA

European Patent Office, P.B. 5818 Patentlaan 2
NL - 2280 HV Rijswijk
Tel. (+ 31-70) 340-2040, Tx. 31 651 epo nl,
Fax (+ 31-70) 340-3016

Authorized officer

Lina, F

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No

PCT/US 94/14335

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
GB-A-2121598	21-12-83	NONE	
US-A-3973146	03-08-76	NONE	
EP-A-0453372	23-10-91	JP-A- 4001535	07-01-92
		JP-A- 4162683	08-06-92
		AU-B- 631734	03-12-92
		AU-A- 7505191	19-12-91
		EP-A- 0604405	29-06-94
		KR-B- 9403274	16-04-94
		US-A- 5118944	02-06-92
US-A-5006711	09-04-91	JP-A- 2098965	11-04-90